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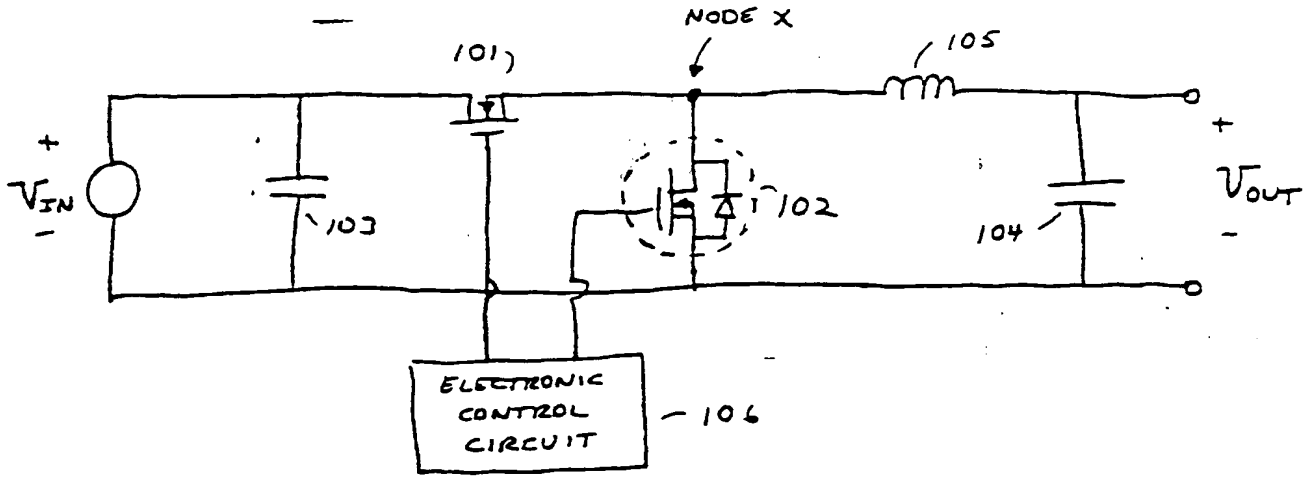

FIG. 1: A NON-ISOLATED DOWN-CONVERTER USING SYNCHRONOUS RECTIFICATION AND AN ACTIVE DRIVE SCHEME.

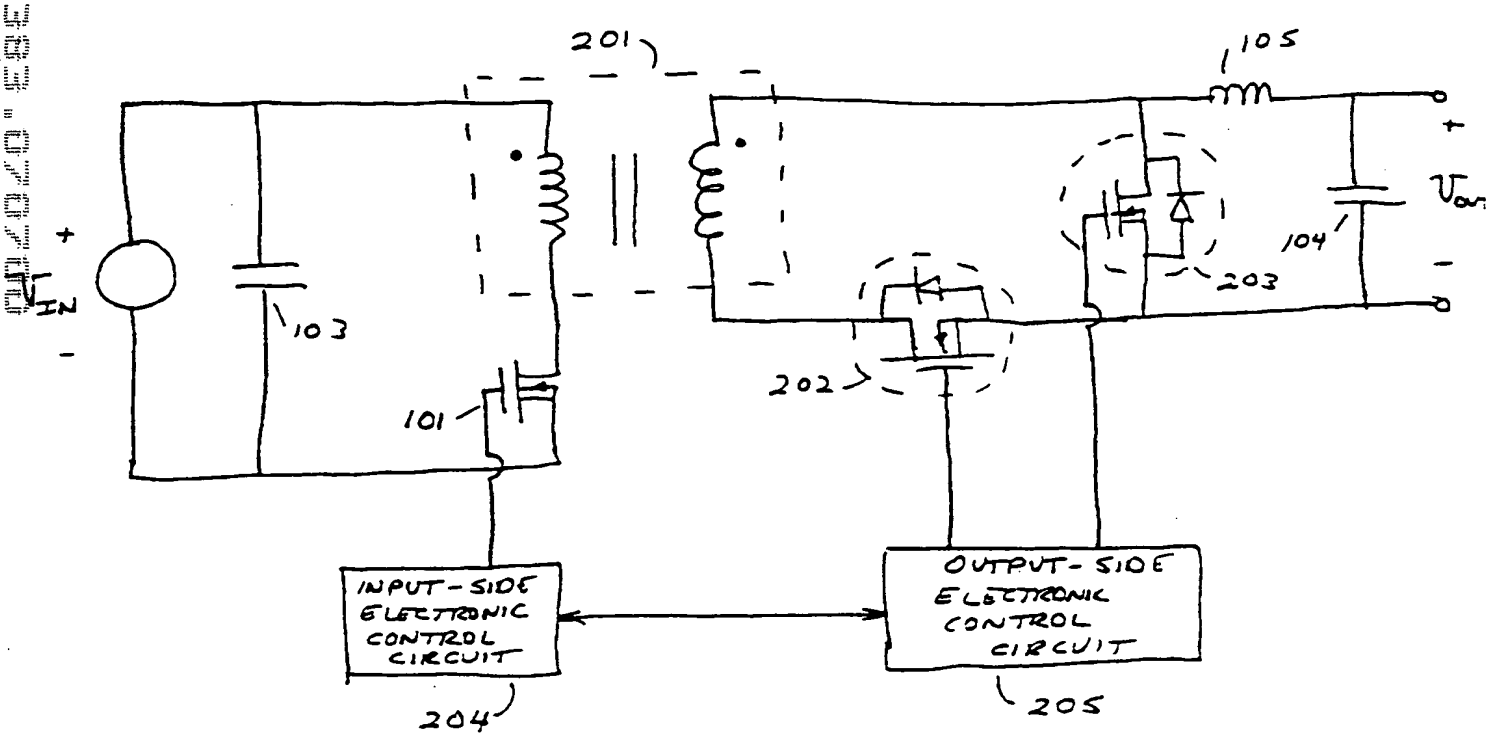

FIG 2: AN ISOLATED FORWARD CONVERTER USING SYNCHRONOUS RECTIFICATION AND AN ACTIVE DRIVE SCHEME

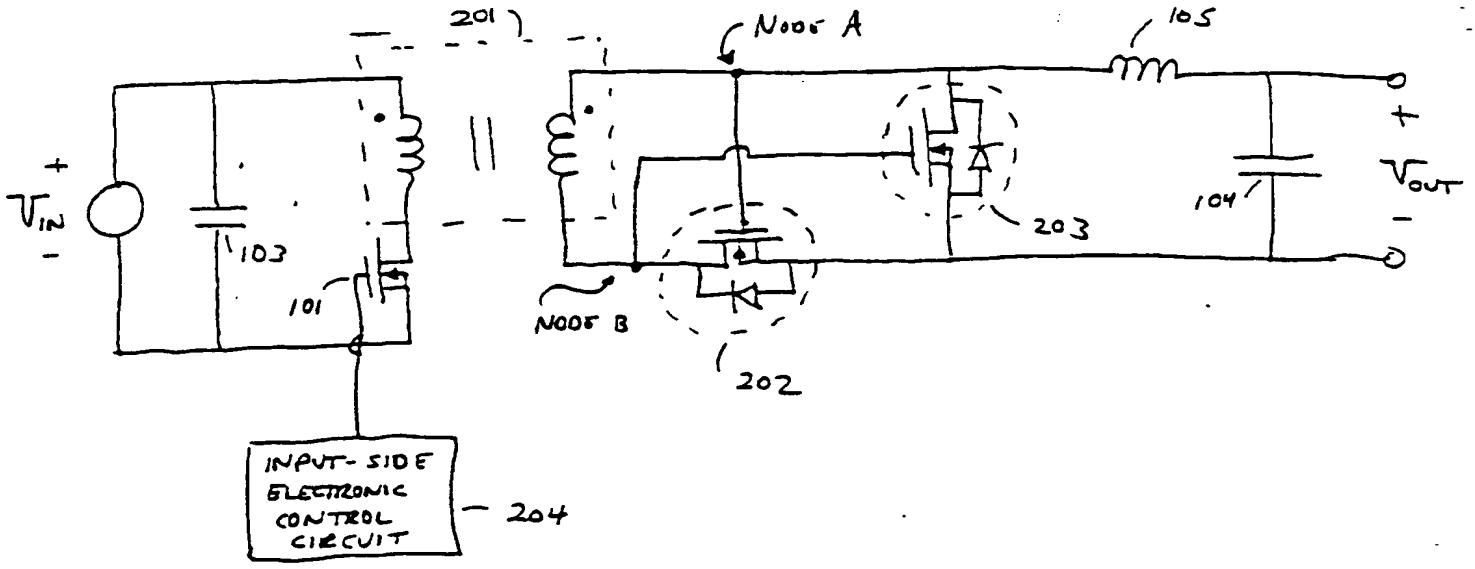

FIG 3: AN ISOLATED FORWARD CONVERTER USING SYNCHRONOUS RECTIFICATION A PASSIVE DRIVE SCHEME.

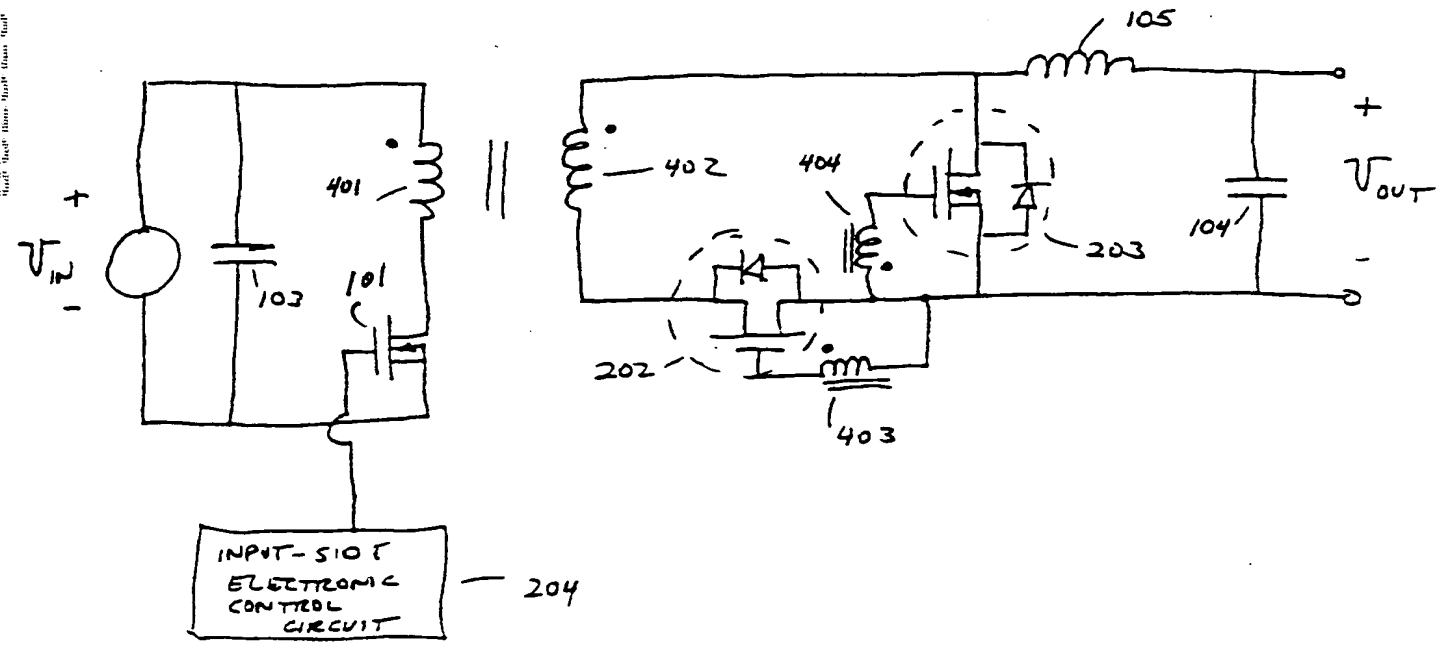

FIG 4: AN ISOLATED FORWARD CONVERTER WITH THE SYNCHRONOUS RECTIFIERS DRIVEN BY AUXILIARY TRANSFORMER WINDINGS.

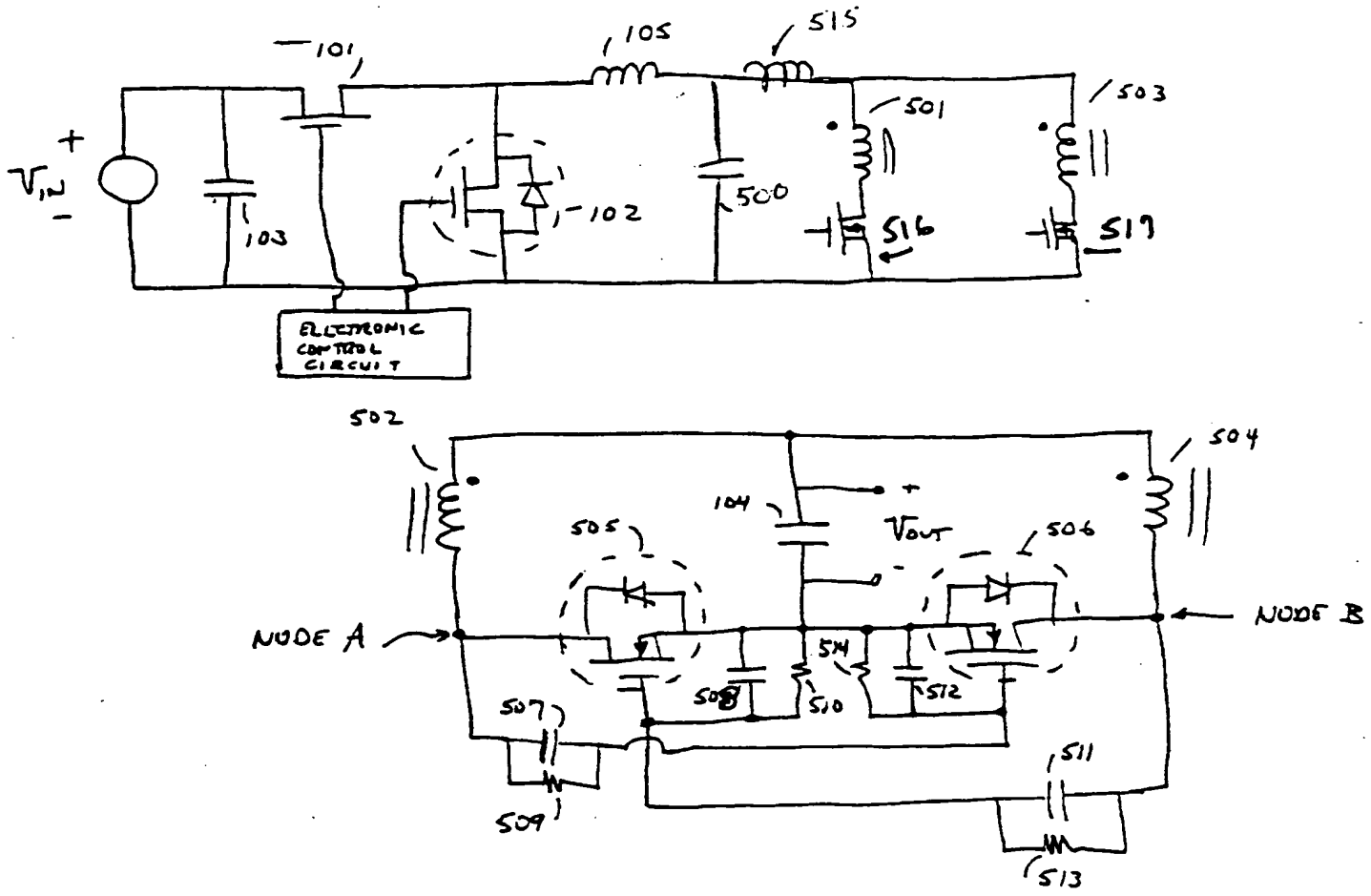

FIG 5: ANOTHER ISOLATED DC/DC CONVERTER USING SYNCHRONOUS RECTIFIERS DRIVEN THROUGH PASSIVE CIRCUITRY.

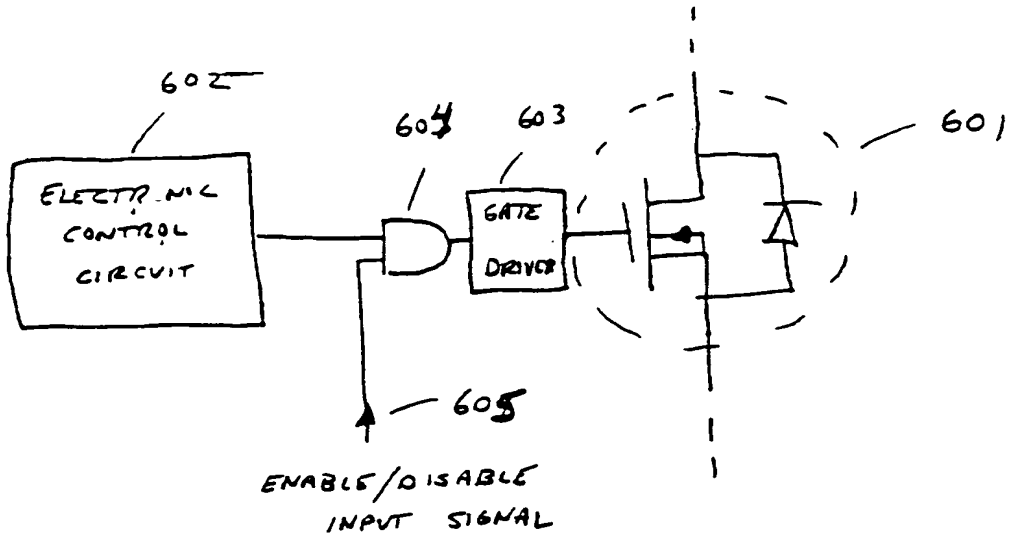

FIG. 6: INSERTION OF A LOGIC GATE IN AN ACTIVE DRIVE CIRCUIT TO ENABLE/DISABLE A SYNCHRONOUS RECTIFIER.

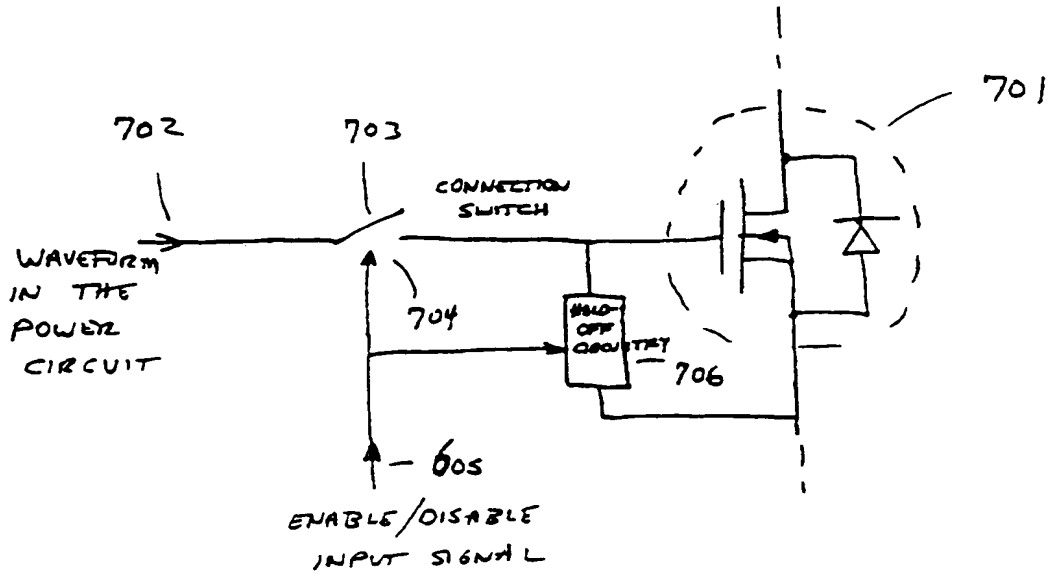

FIG 7: INSERTION OF A CONNECTION SWITCH AND A HOLD-OFF CIRCUITRY IN A PASSIVE GATE DRIVE CIRCUIT TO ENABLE/DISABLE A SYNCHRONOUS RECTIFIER.

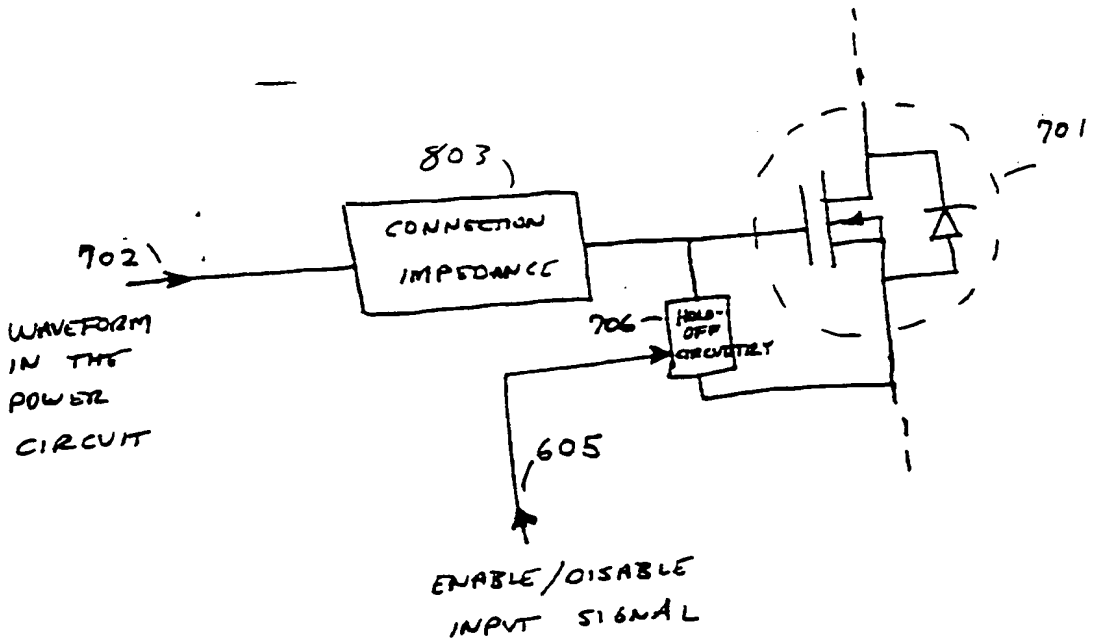

FIG. 8: INSERTION OF A CONNECTION IMPEDANCE AND A HOLD-OFF CIRCUITRY IN A PASSIVE GATE DRIVE CIRCUIT TO ENABLE/DISABLE A SYNCHRONOUS RECTIFIER.

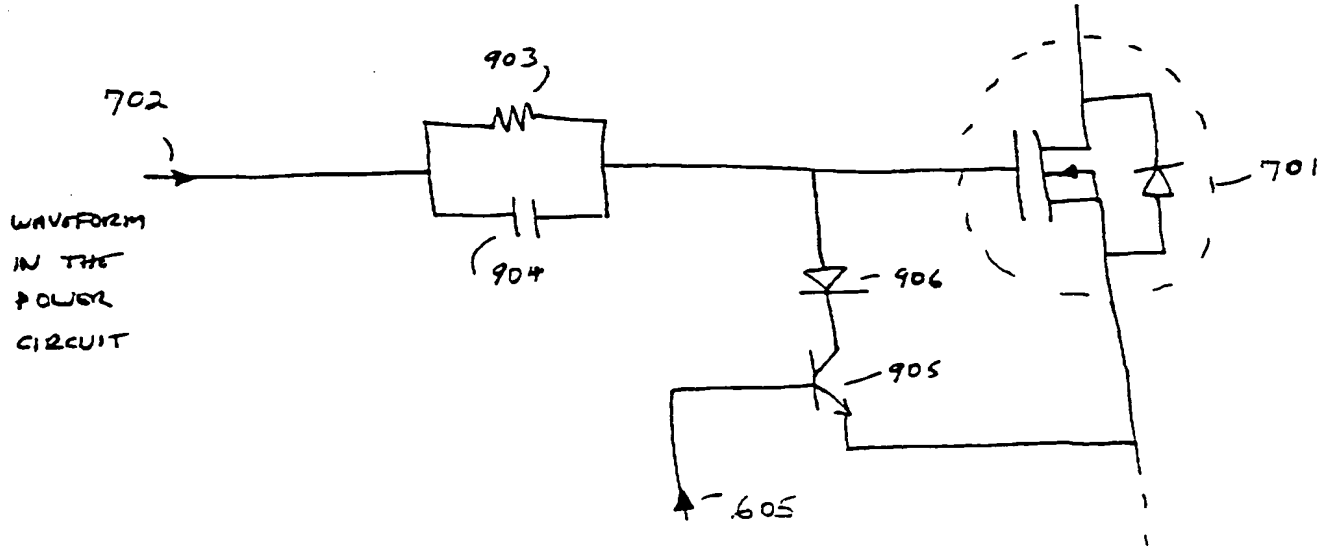

FIG. 9: A SPECIFIC IMPLEMENTATION OF THE CONCEPTS DEPICTED IN FIG. 8.

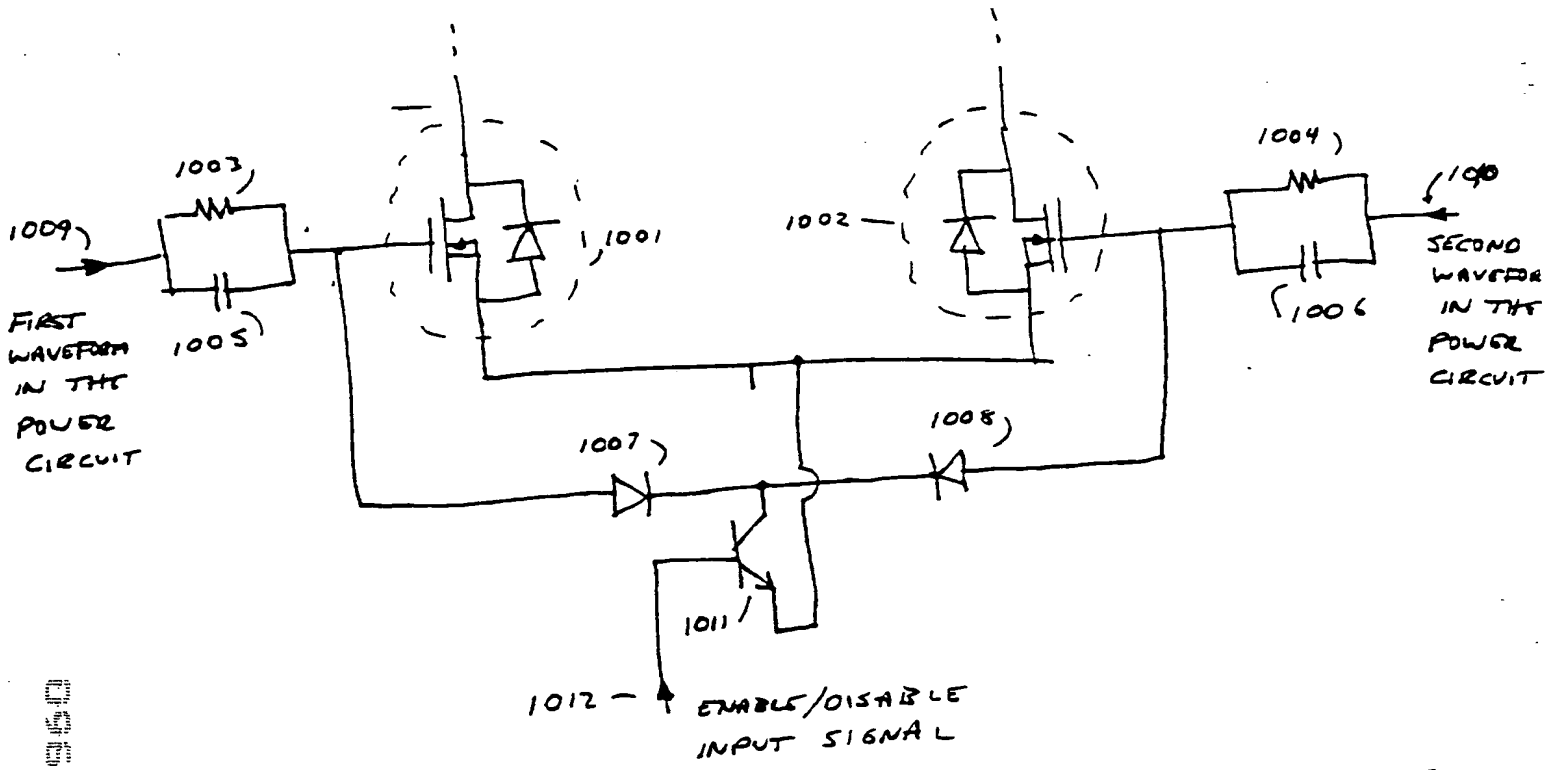

FIG. 10: THE IMPLEMENTATION OF FIG 9 MODIFIED SUCH THAT ONLY ONE TRANSISTOR IS USED IN THE HOLD-OFF CIRCUITRY FOR TWO SYNCHRONOUS RECTIFIERS.

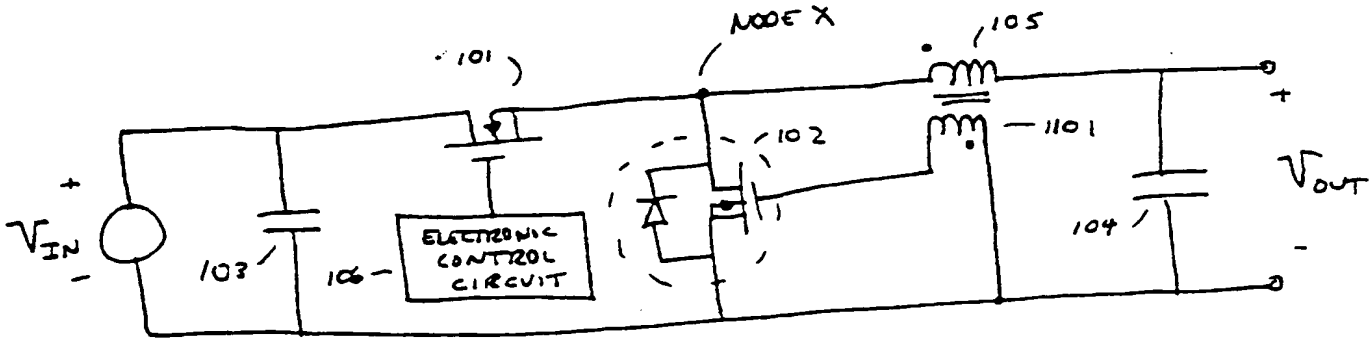

FIG. 11 A NON-ISOLATED DOWN-CONVERTER USING SYNCHRONOUS RECTIFICATION AND A PASSIVE DRIVE.

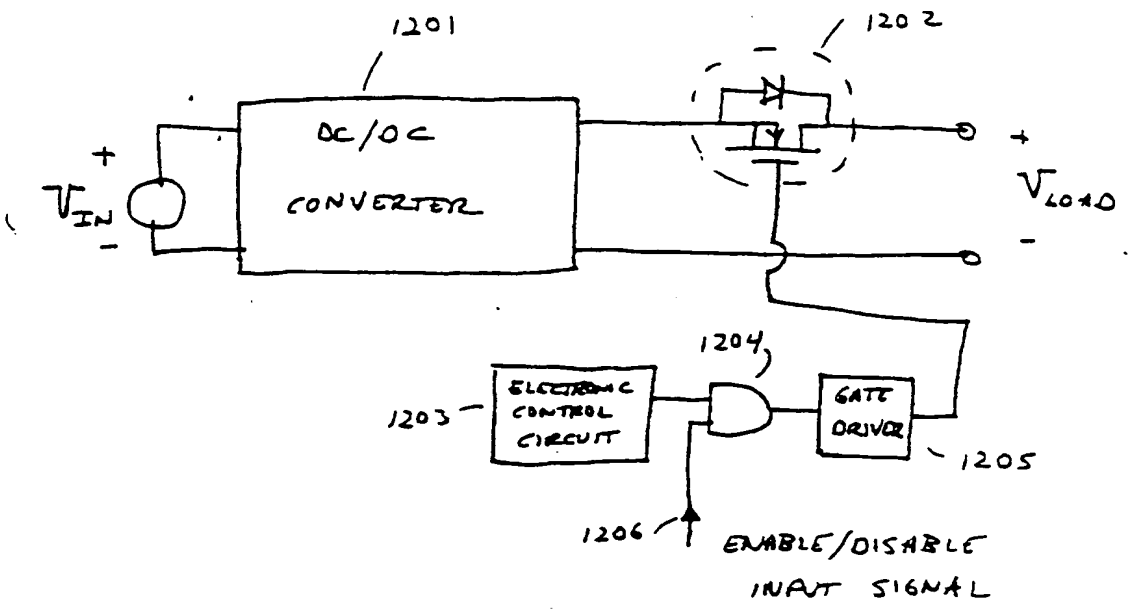

FIG 12: AN ORING TRANSISTOR DRIVEN BY AN ACTIVE CONTROL CIRCUIT WITH A LOGIC GATE TO PROVIDE THE ENABLING/DISABLING FUNCTION.

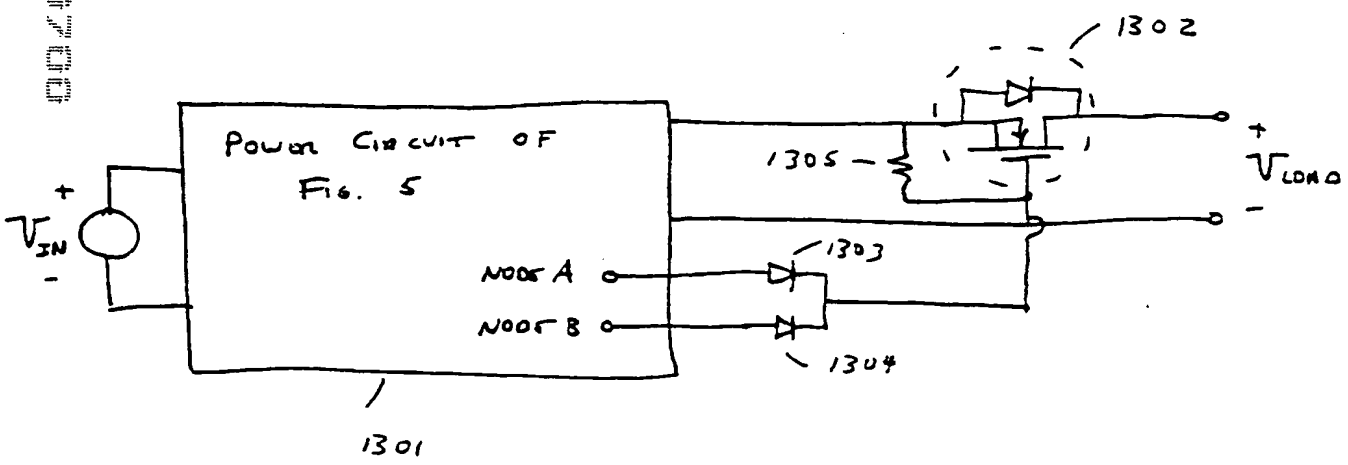

FIG. 13: AN ORING TRANSISTOR DRIVEN BY WAVEFORMS IN THE POWER CIRCUIT SHOWN IN FIG. 5.

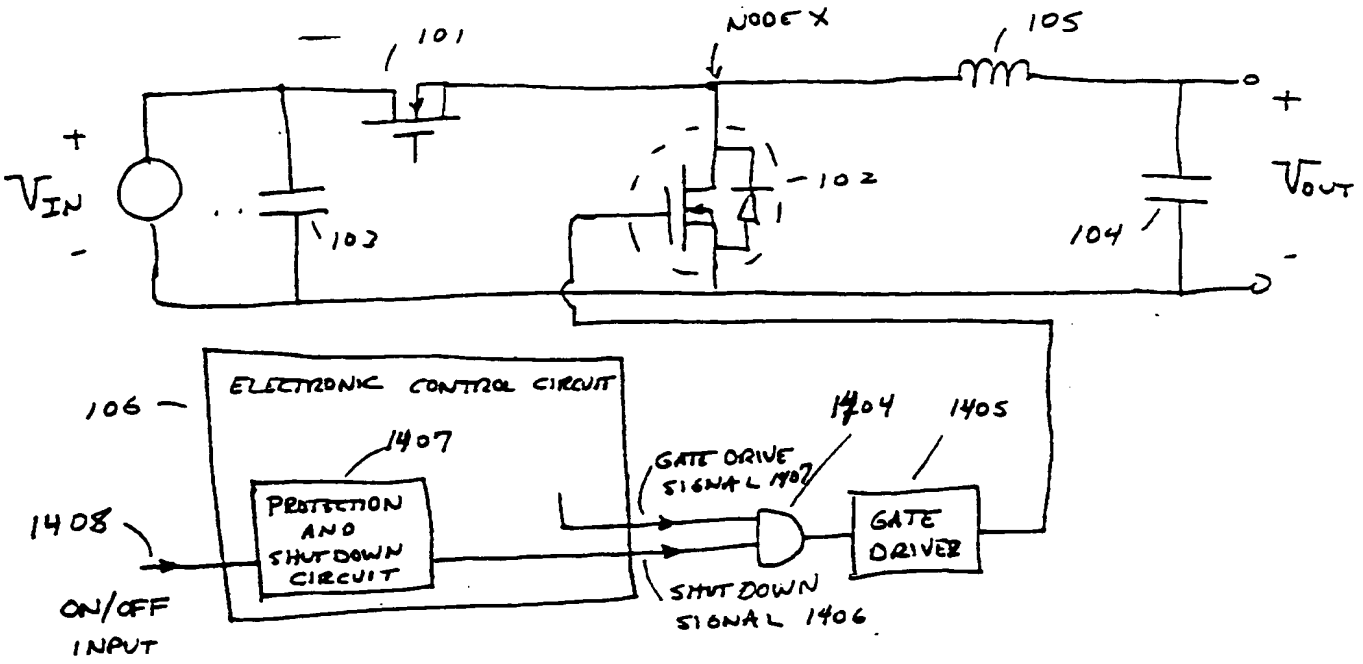

FIG. 14: DERIVING THE ENABLE/DISABLE SIGNAL FROM THE CONTROL CIRCUIT'S SHUTDOWN SIGNAL

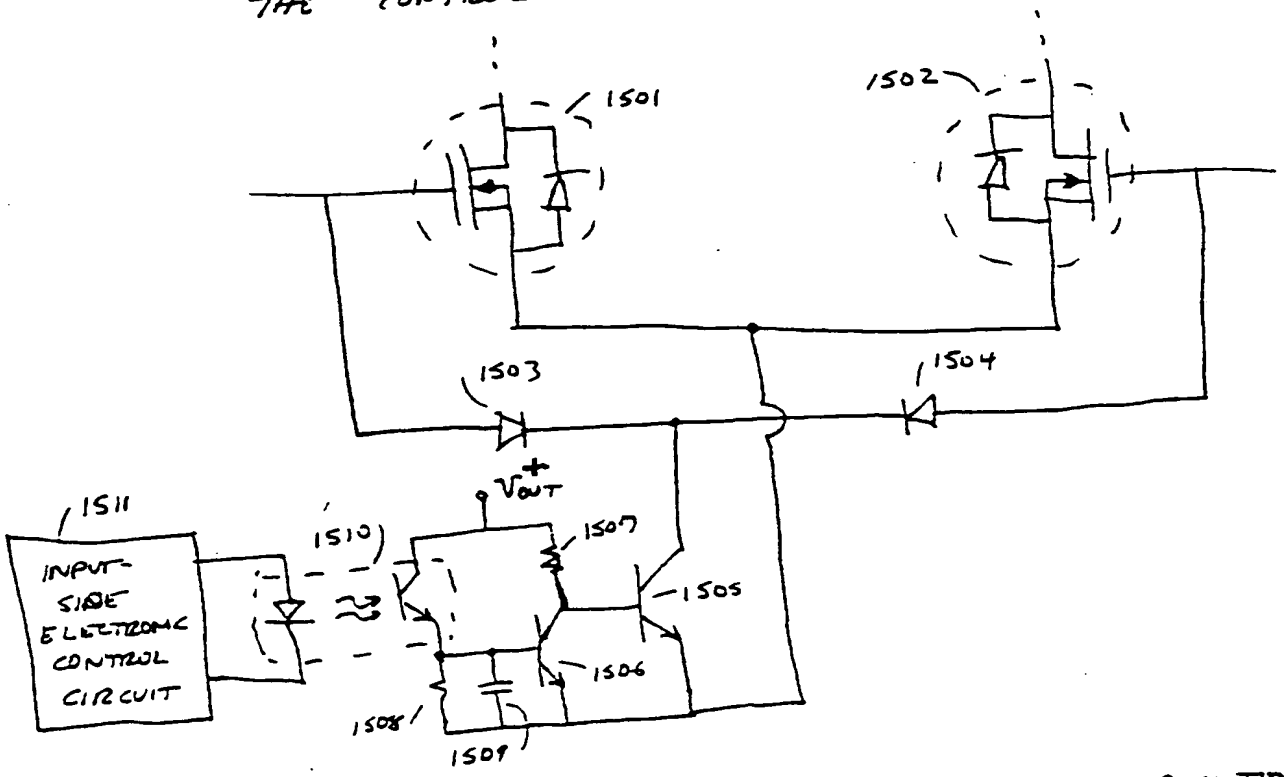

FIG 15: A SPECIFIC IMPLEMENTATION OF THE CONCEPT DEPICTED IN FIG. 9 IN WHICH AN OPTO-ISOLATOR IS USED TO CONVEY THE ENABLE/DISABLE INPUT SIGNAL FROM ~~THE INPUT~~ SIDE CONTROL CIRCUIT.

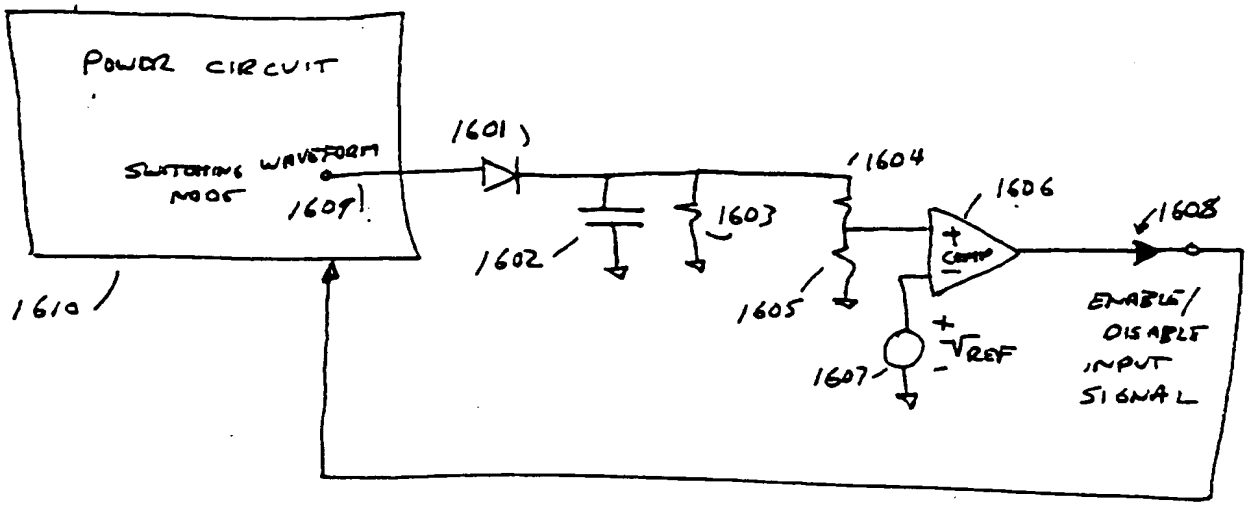

FIG 16: USING A SWITCHING WAVEFORM IN THE POWER CIRCUIT TO INDICATE THAT THE CONVERTER HAS BEEN SHUTDOWN TO PROVIDE A "SHUTDOWN DECISION LOGIC SIGNAL".

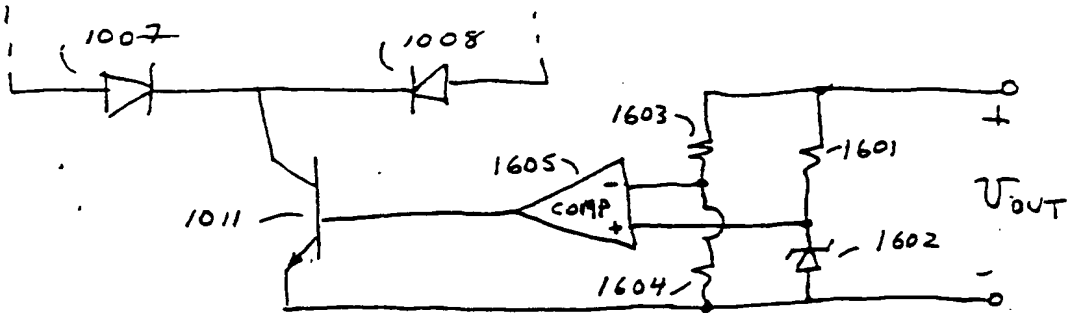

FIG. 17: USING A COMPARITOR CIRCUIT TO DETECT THAT THE OUTPUT VOLTAGE IS TOO LOW AND TO DISABLE THE SYNCHRONOUS RECTIFIERS.

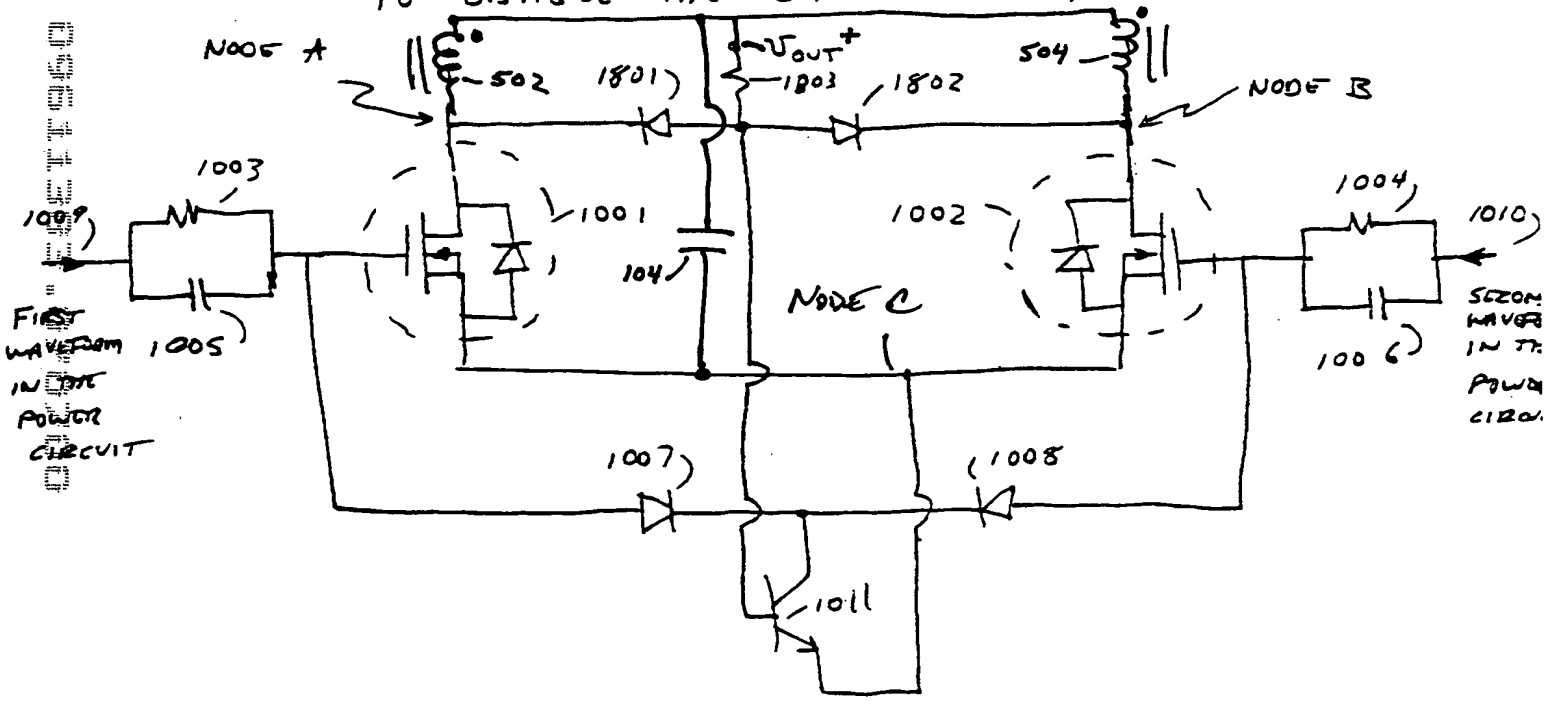

FIG 18: SENSING OUTPUT CURRENT DIRECTION INDIRECTLY THROUGH THE VOLTAGE DROP ACROSS THE SYNCHRONOUS RECTIFIERS.

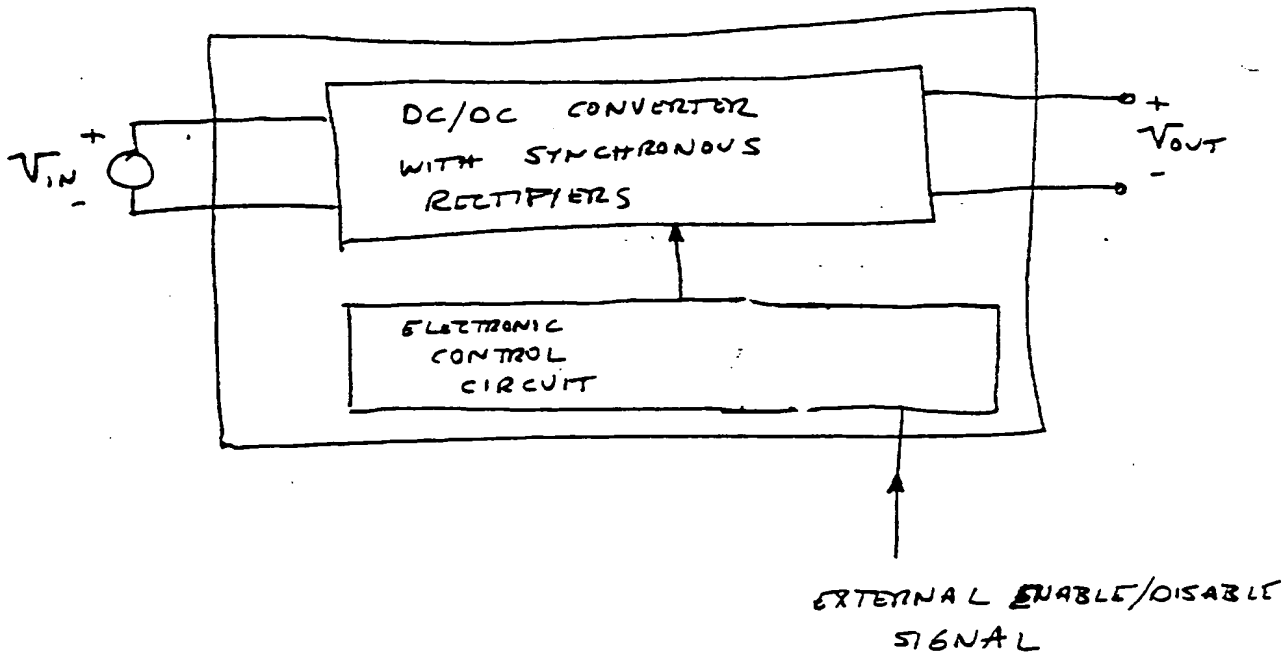

FIG. 19: A DC/DC CONVERTER USING SYNCHRONOUS RECTIFIERS IN WHICH THE DECISION TO ENABLE/DISABLE THE RECTIFIERS IS PROVIDED BY AN EXTERNALLY SUPPLIED SIGNAL

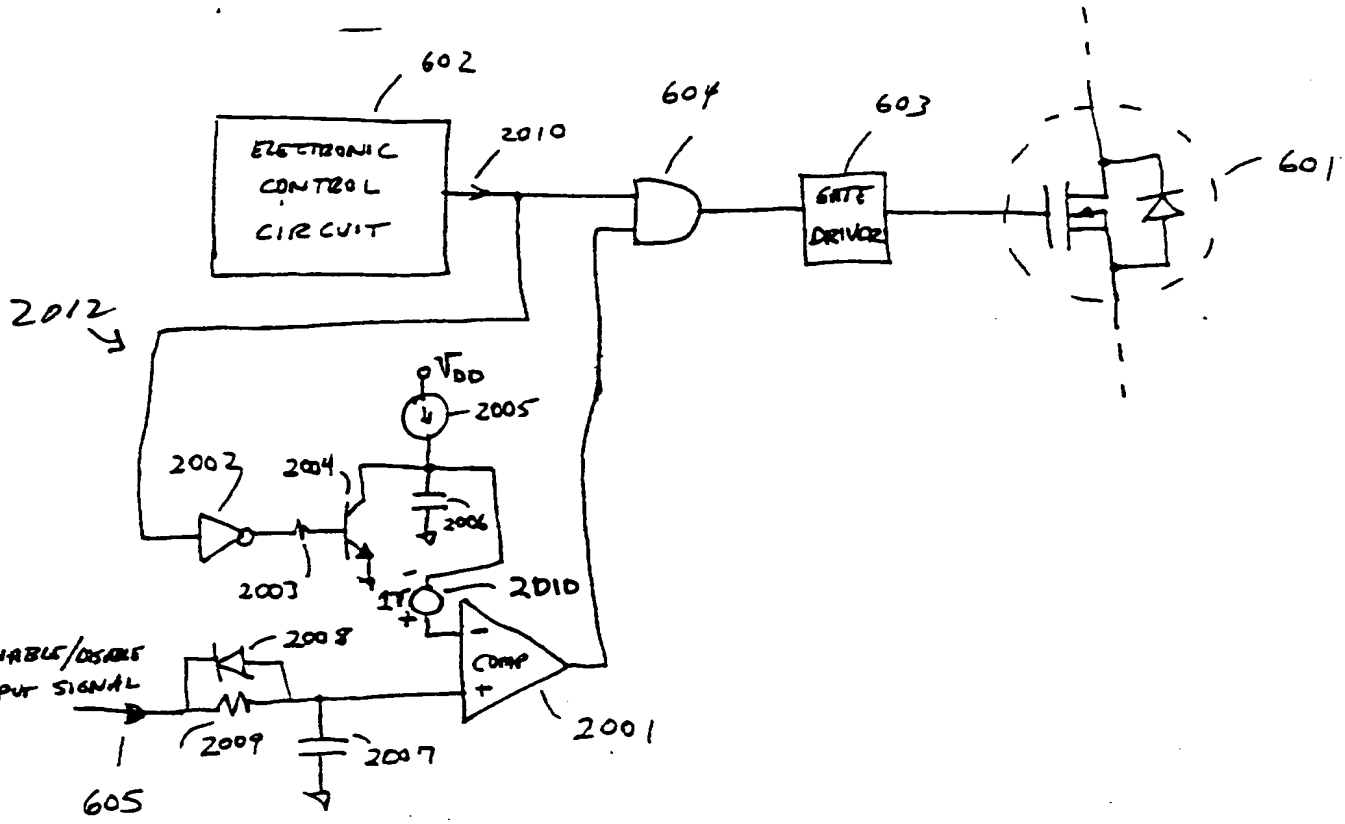

FIG. 20: SLOWLY ENABLING A SYNCHRONOUS RECTIFIER BY GRADUALLY INCREASING ITS ON-STATE DURATION DURING ITS NORMAL CONDUCTION INTERVAL.

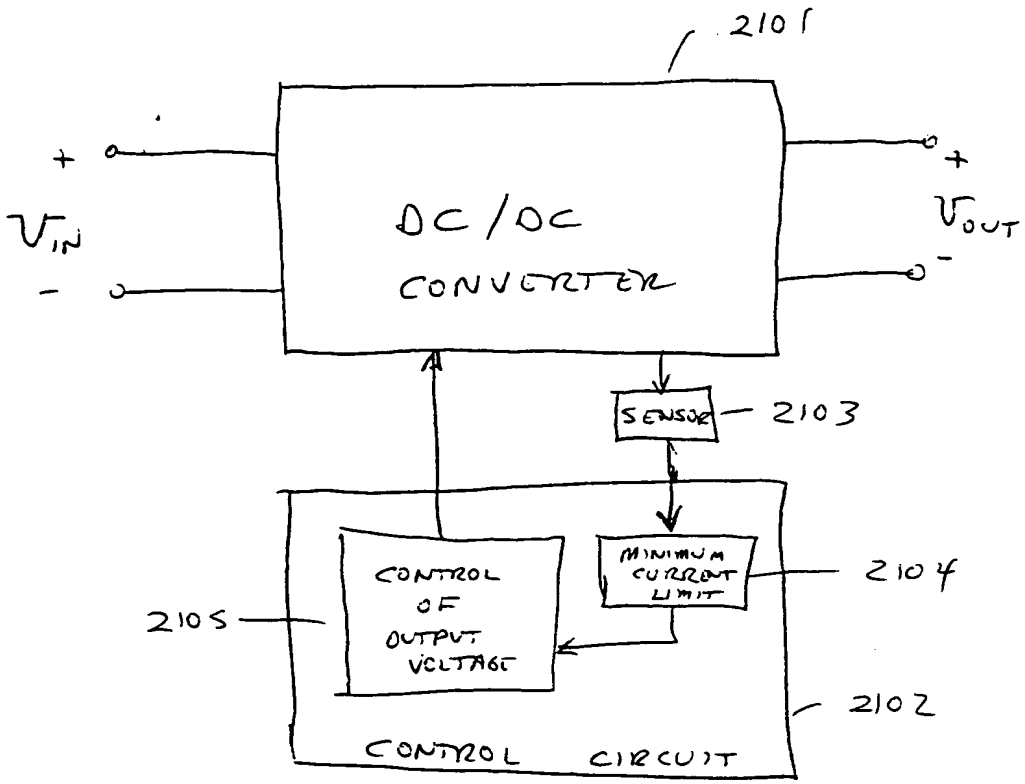

FIGURE 21: BLOCK DIAGRAM SHOWING DC/DC CONVERTER CONTROL CIRCUIT WITH A MINIMUM CURRENT LIMIT

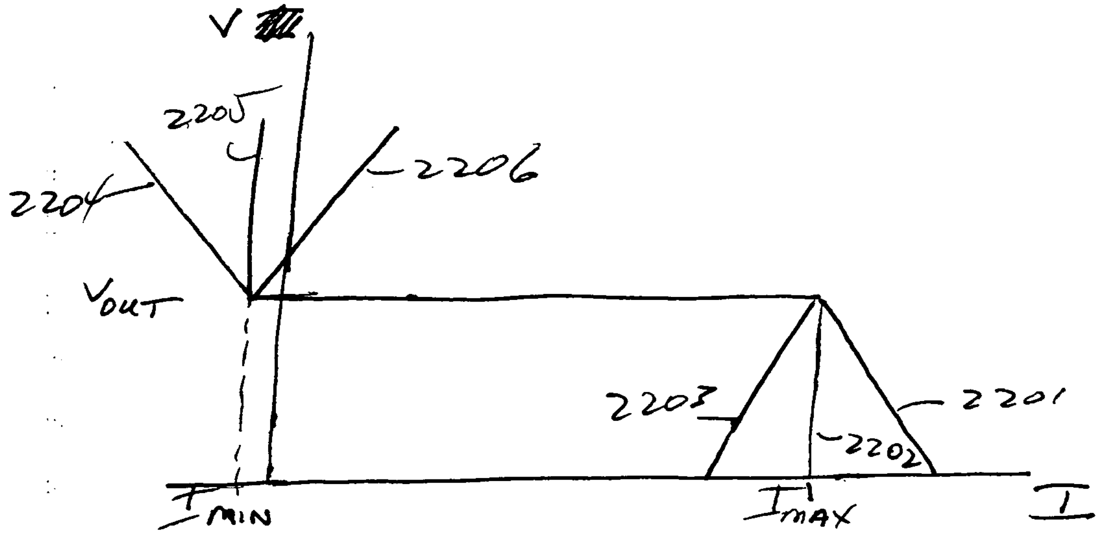

FIG 22

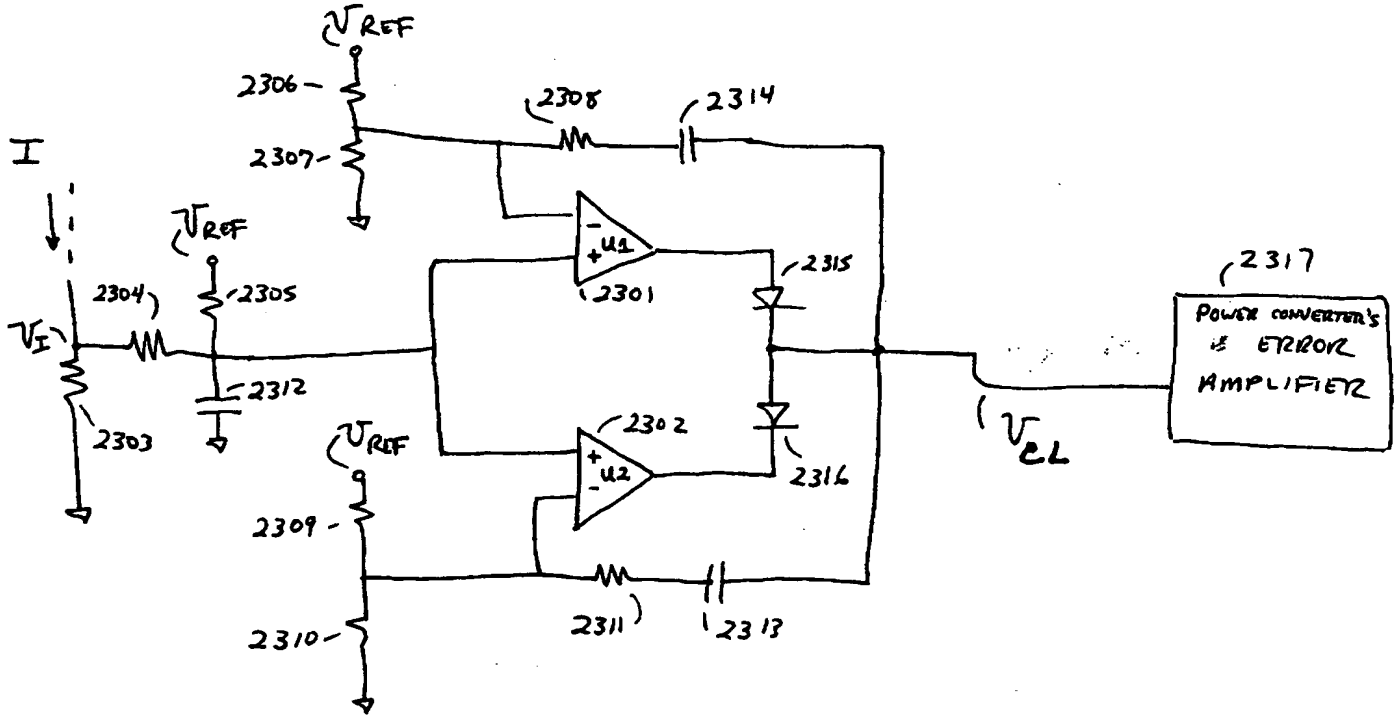

FIGURE 23: ONE METHOD TO IMPLEMENT BOTH A MAXIMUM AND A MINIMUM CURRENT LIMIT.